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EXAMINER
ENGLUND, TERRY LEE

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/769,534	AKIYOSHI, HIDEO	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

The request for continuation, preliminary amendment, and formal drawings submitted on Aug 22, 2002 have been reviewed and considered with the following results:

The continuation request was approved and entered.

The formal drawing of Fig. 2 was also approved. It shows "PORL" instead of --PROL-- shown in the original Fig. 2.

Amended claims 2, 4, and 6 overcame their respective objection described in the previous Office Action. Therefore, those objections have been withdrawn.

Since independent claims were not amended, and the comments did not overcome the prior art rejections described in the previous Office Action, those rejections have been maintained. The rejections are repeated below under the appropriate section, with some minor modifications. The examiner's comments, with respect to the applicant's comments and arguments, are given in the Response to Arguments section.

All of the newly added claims 8-17 have their own respective rejections described below under the appropriate section(s).

Claim Rejections under 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8, 11, 14 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The transistor/threshold voltage limitations recited within claims 8 and 11 are confusing and/or misleading. It is not clear how the plurality of sub power-on reset signals relate to the single "the threshold voltage" recited on line 3-4 of claim 8. For example, is each of the plurality of signals based on the same transistor, and thus the same threshold voltage? Similarly, it appears each of the plurality of signals on line 2 of claim 11 is generated according to a single threshold voltage of one transistor. However, it is believed there is a respective transistor and threshold voltage for each signal as shown/disclosed by the applicant. Line 4 of both claims 14 and 16 implies the pulses are generated on the basis of a single signal (e.g. the sub power-on reset signal or the external power-on reset signal). However, doesn't each pulse correspond to a respective reset signal, and not just one of them?

Claim Rejections under 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-7 remain rejected, and new claims 8-11 are rejected, under 35 U.S.C. 102(e) as being anticipated by Malherbe, a reference cited in previous Office Actions. The invention of Malherbe provides a power-on reset means for an internal circuit (e.g. not shown but related to the disclosed "functional electronic circuit" on column 3, lines 56-65). In Fig. 3, Malherbe shows an integrated circuit comprising a sub reset signal generator CE1-CEn for generating a plurality of sub power-on reset signals POR1-PORn; and a main reset signal generator OR for generating a main power-on reset pulse signal POR that is used to initialize (related to the "an inhibiting means" disclosed on column 3, line 66 through column 4, line 15, and column 5, lines 7-10) the internal circuit according to the sub power-on reset signals POR1-PORn. Sine the main pulse signal POR is in response to the sub power-on reset signals POR1-PORn, it is understood signal POR is generated "according to at least one from any of said sub power-on reset signals." One of ordinary skill in the art would know from Malherbe's disclosure that once the "inhibiting means" is deactivated, the internal circuit will be allowed to operate (e.g. turn on) because a sufficient power supply voltage is available for efficient operation. Fig. 4 shows details of each sub reset signal generator CE1-CE3 (corresponding to CE1-CEn of Fig. 3). Since each generator has its own unique configuration, their respective sub power-on reset signal (i.e. POR1-PORn shown in Fig. 3) will have a different timing than the other sub power-on reset signals, anticipating claim 1. Fig. 3 also shows a reset terminal (unlabeled) for receiving an external power-on reset signal TPOR, thus anticipating claims 3 and 5. Referring to Fig. 4, and interpreting the circuit differently, the sub reset signal generator is deemed the elements

10-13,20-23,30-34 which generate a plurality of sub power-on reset signals (e.g. the outputs of 12/13; 22/23; and 33/34) at different timings (due to the different configurations of the elements). The main reset signal generator comprises elements 15,16,24,33,36,OR for generating a main power-on reset signal POR in response to the sub power-on reset signals, thus anticipating claim 1 also. Since the main reset signal generator comprises a plurality of pulse generators (i.e. 15/16, 24, and 35/36) for generating pulses on the basis of a transition edge of a corresponding sub power-on reset signal, and a composite circuit OR for generating the main power-on reset signal POR, claim 2 is anticipated. [It is noted each pulse generator (in this case, at least one inverter) will generate a pulse in synch with a transition edge of a respective sub power-on reset signal. For example, when the rising edge of the voltage (sub power-on reset signal) from 12/13 reaches the switching threshold of inverter 15, pulse generator 15,16 will provide an associated transition pulse.] Using the same type of reasoning as applied above, elements 50,51 of Fig. 5 are deemed a means for providing an external power-on reset signal to reset terminal - (of comparator 52), and comparator 52 can be deemed one of the plurality of pulse generators. Therefore, composite circuit OR generates the main power-on reset signal POR in response to the sub power-on reset signal(s) and the external power-on reset signal, anticipating claims 4 and 6. When considering Figs. 3-5, one of ordinary skill in the art would recognize 15/16, 24, 35/36, and 52 generate a plurality of power-on reset pulse signals (i.e. POR1, POR2, PORn, and TPOR, respectively) according to a plurality of sub power-on reset signals (from 10-13, 20-23, 30-34, and 50/51, respectively), and OR initializes an internal circuit (not

shown, but previously described above) by signal POR according to (at least one of) the power-on reset pulse signals. Therefore, claim 7 is also anticipated. Without repeating most of the details previously described, new claims 8-11 will now be addressed. Since sub reset signal generator CE1-CE3 of Fig. 4 includes at least transistors 10, 20, and 30 (having their own respective threshold voltage), the corresponding sub power-on reset signals POR1-PORn (shown in Fig 3) will be generated based on their respective transistor's threshold voltages, anticipating claim 8. Deeming CE1 as a first sub reset signal generator with first transistor 10 having a first threshold voltage, it generates a first sub-power-on reset signal POR1 (see Fig. 3) based on the first threshold voltage, and deeming CE2 as a second sub reset signal generator with second transistor 20 having a second threshold voltage, it generates a second sub-power-on reset signal POR2 (see Fig. 3) based on the second threshold voltage. Since main reset signal generator OR generates main power-on reset signal/ pulse POR, claim 9 is anticipated. Re-identifying elements 10-13,20-23,30-34 as a sub reset signal generator for generating a plurality of sub power-on reset signals at different timings; 15,16, 24, and 35,36 as a plurality of pulse generators for generating pulses based on the sub power-on reset signals; and OR as the composite circuit for synthesizing the pulses to generate main power-on reset signal POR, claim 10 is anticipated. Elements 10-13,20-23,30-34 generate a plurality of sub power-on reset signals according to the threshold voltage of a transistor (e.g. transistor 10 within 10-13; transistor 20 within 20-23; and transistor 30 within 30-34) at different timings; elements 15,16, 24, and 35,36 generate a plurality of pulse signals according to the sub power-on reset signals; and OR

initializes an internal circuit (not shown, but understood from the disclosure and knowledge of one of ordinary skill in the art) according to at least one of the power-on reset signals, anticipating 11.

Claims 1-3, 5, and 7 also remain rejected, and new claims 8-12, and 17 are rejected, under 35 U.S.C. 102(e) as being anticipated by Crotty, another reference cited in previous Office Actions. Crotty shows a circuit in Fig. 6 with blocks 630,640,650,210, 220 closely corresponding to blocks 10,16,20,12,18, respectively of the applicant's own Fig. 1. [For example, Crotty's block 630 is shown in detail in Fig. 8(a). It is similar to sub generator block 10 (12) of the applicant's Fig. 1, and shown in detail in the applicant's Fig. 2, wherein both comprise a type of voltage divider/detector with its output being applied to at least one inverter. Examples of Crotty's blocks 220 and 650 are shown in Figs. 4(a) and 7, respectively. These blocks/details correspond to details of blocks 16 and 20 shown in the applicant's Fig. 1.] Fig. 6 shows a sub reset signal generator 630,210 for generating a plurality of sub power-on reset signals VD2,VD1; and a main reset signal generator 640,220,650 for generating a main power-on reset pulse signal POR according to at least one of the sub power-on reset signals. Signal POR is used to initialize an internal circuit (not shown but disclosed as logic circuits or IC devices (e.g. see column 1, lines 6-31)). Since the configurations of circuits 630 and 210 are different from each other (e.g. see details of 630 in Fig. 8(a), and of 210 in Figs. 3(a) and 3(d)), their respective reset signals VD2 and VD1 will have different timings from each other, thus anticipating claim 1. The main reset signal generator 640,220, 650 comprises a plurality of pulse generators 640,220 and a composite circuit 650. Each pulse generator

640,220 of Crotty could be configured as shown in Fig. 4(a), with details of the delay circuit 420 shown in Fig. 5(a). Deeming inverters 512-516 of Fig. 5(a) a delay in series with inverter 518, each pulse generator 640,220 of Crotty corresponds to the pulse generators 16,18 shown in the applicant's own Fig. 1, wherein each pulse generator of Crotty comprises a delay 22, inverter 24, and NAND gate 26. Fig. 7 of Crotty shows details of block 650. It comprises a NAND gate and inverter coupled in series, wherein the NAND gate receives the POR1,POR2 signals and generates signal POR. Therefore, claim 2 is also anticipated. Blocks 640,220 generate a plurality of power-on reset pulse signals POR2,POR1 according to a plurality of sub power-on reset signals VD2,VD1, and block 650 initializes an internal circuit (not shown, but previously described) according to at least one of the power-on reset signals POR2,POR1, anticipating claim 7. Fig. 10 of Crotty shows another embodiment of the circuit. This embodiment comprises a sub reset signal generator 630,210,930 for generating sub power-on reset signals POR2,POR1; a reset terminal (not labeled) for receiving an external power-on reset signal POR3; and a main reset signal generator 1010 for generating a main power-on reset signal pulse POR. Therefore, applying the same type of reasoning as previously described (with respect to different timings, and the initialization of an internal circuit according to at least one reset signal), claims 3 and 5 are also anticipated. [Also, it is noted that Crotty discloses main reset signal generator 1010 transitions main signal POR "if one or more of power on reset signals POR1, POR2, and POR3 are in the power-off logic level" (see column 11, lines 6-13). This disclosure thus provides support of the "at least one" related limitations within the claims.] Without repeating most of the

obvious structural relationships previously described, the rejections of new claims 8-12, and 17 will now be considered. Since sub reset signal generator can include blocks 630 and 210 (shown in Fig. 6), wherein block 630 includes at least one transistor (e.g. 810 shown in Fig. 8(a)) having a threshold voltage, and block 210 includes at least one transistor (e.g. 310 shown in Fig. 3(a)), the sub reset signal generator of Crotty will generate the plurality of sub power-on reset signals POR2 and POR1 based on the threshold voltages, anticipating claim 8. When blocks 630,640 are deemed a first sub reset signal generator, it includes a first transistor (e.g. 810) having a first threshold voltage, and providing first sub power-on reset signal POR2 based on the first threshold hold voltage. Also, blocks 210,220 can be deemed a second sub reset signal generator including a second transistor (e.g. 310) having a second threshold value, and providing second sub power-on reset signal POR1 based on the second threshold value. Therefore, claim 9 is anticipated. Deeming blocks 630 and 210 as the sub reset signal generator, blocks 640,220 as a plurality of pulse generators, and block 650 as the composite circuit, claim 10 is anticipated. Since blocks 630 and 210 generate a plurality of sub power-on reset signals VD2 and VD1 according to a threshold voltage of a transistor (e.g. see 810 in Fig. 8(a) and 310 in Fig. 3(a)) with different timings; blocks 640 and 220 generate a plurality of pulse signals POR2 and POR1 according to the sub power-on reset signals; and block 650 initializes an internal circuit (not shown, but understood from the disclosure and knowledge of one of ordinary skill in the art), method claim 11 is anticipated. Although the reference of Crotty does not show waveforms of pulses POR2 and POR1, they are considered shorter than an interval

between transition edges of the sub power-on reset signals VD2,VD1 because of their structural/functional equivalency with respect to the applicant's own circuits, thus anticipating claim12. [For example, each pulse generator 640,220 of Crotty has a functionally equivalent structure as the applicant's own pulse generators. Crotty's Fig. 4(a) is an example of a circuit that can be used as pulse generator 220 and/or 640 of Crotty's Fig. 6 (e.g. sub power-on reset signal VD1 is received at an input, and pulse POR1 is provided at the output). Figs. 4(a)/5(a) of Crotty will now be compared to pulse generator 16 (which also has the same structure as pulse generator 18) shown in the applicant's Fig. 1. Although Crotty shows a delay line circuit 420 in Fig. 4(a), it is shown in more detail in Fig. 5(a). Inverters 512-516 of Crotty can be deemed a delay. The Fig. 4(a) pulse generator of Crotty then has NAND gate 410 receiving signal VD1 directly, and indirectly through delay 512-516 and inverter 518. This structure corresponds to the applicant's NAND gate 26 receiving signal PORH directly, and indirectly through delay 22 and inverter 24. Therefore, the circuits are considered structurally identical, and their functions will also be the same. If the pulse generators (e.g. 16,18) of the applicant generate pulses shorter than the interval between transition edges of the sub power-on reset signals, then the pulse generators 640,220 of Crotty will also generate the shorter pulses.] Also, by using this type of reasoning, blocks 630,640,210,20 generate a plurality of power-on reset signals/pulses POR2, POR1 with different timings and having the shorter interval, while block 650 initializes an internal circuit according to at least one of the power-on reset signals, anticipating claim 17.

Claim Rejections 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malherbe. Fig. 3 of Malherbe shows a sub reset signal generator CE1-CEn for generating a plurality of sub power-on reset signals POR1-PORn having different timings; a reset terminal (not labeled) for receiving an external power-on reset signal TPOR from external circuit DET; and a main reset signal generator OR for generating main power-on reset signal/pulse POR according to at least one of the sub power-on reset signals and external power-on reset signal. However, the reference does not clearly show or disclose the external power-on reset signal TPOR being supplied from the exterior of the IC. It would have been obvious to one of ordinary skill in the art to position temperature detector DET, which provides signal TPOR, either on, or exterior, to the semiconductor IC. With detector DET positioned off the IC, claims 13 and 15 are rendered obvious. Detector DET could be located away from the IC in order to better monitor the temperature of other circuits/ elements, which could be more temperature sensitive than the IC containing the sub reset signal generator and main reset signal generator. Since the main reset signal generator can be considered pulse generators CE1-CEn and composite circuit OR, it comprises a plurality of pulse generators that generate pulses bases on the transition

edge of at least one of the sub power-on reset signals, and the composite circuit for synthesizing the pulses to generate the main power-on reset signal POR, rendering obvious claims 14 and 16.

In so far as being understood, claims 13-16 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Crotty. Fig. 6 of Crotty shows a sub reset signal generator 630,640,210,220 for generating a plurality of sub power-on reset signals POR2,POR1 having different timings; and a main reset signal generator OR for generating main power-on reset signal/pulse POR according to at least one of the sub power-on reset signals. Although Fig. 6 does not show a reset terminal for receiving an external power-on reset signal, that is shown in Fig. 10 wherein external circuit 1020 provides an external power-on reset signal POR3 to main reset signal generator 1010. However, the reference does not clearly show or disclose the external power-on reset signal POR3 being supplied from the exterior of the IC, or to main reset signal generator 650 of Fig. 6. It would have been obvious to one of ordinary skill in the art to modify Fig. 6 by adding Fig. 10's external power-on reset signal POR3 to a three input version of main reset signal generator 650. As shown in Fig. 10, signal POR3 relates to a memory test circuit. This signal could be supplied from the semiconductor IC's exterior, thus rendering claims 13 and 15 obvious. Signal POR3 would be one means, external to the IC, for indicating if a supply voltage is sufficient for writing logic high and logic low into a memory cell (e.g. see column 11, lines 6-13). Since the main reset signal generator could be considered as comprising pulse generators 640,220, and composite circuit 650 as previously described, claims 14 and 16 are also rendered obvious.

No claim is allowable.

Although not used in any formal rejections described above, the references cited on the accompanying PTO-892 should be carefully reviewed and considered. Feddeler et al. shows and discloses a power-on reset circuit/means. For example, when considering Fig. 6, either the output CHIP RESET SIGNAL or the output of NAND gate 86 could be deemed the main power-on reset signal according to at least one of a plurality of input signals (e.g. from RESET PIN 54, an external POWER ON RESET, and OTHER SOURCES OF RESET). Also referring to the Fig. 6 circuit, Feddeler clearly discloses that "These other sources of reset may be generated internal or external to data processing system 40" (see column 4, lines 26-32). System 40 is shown in Fig. 2 with only RESET PIN 54 clearly shown external to system 40 and RESET LOGIC 48. However, from the disclosure, one of ordinary skill in the art would understand the other signals previously described could also be received from an external source, thus they can be considered external with respect to the semiconductor IC containing RESET LOGIC 48 and/or system 40. The reference of Smith also shows and discloses a power-on reset type circuit/means. For example, Fig. 6 shows a main reset signal generator 314 (shown in detail in Fig. 7) receiving a plurality of sub power-on reset signals/pulses from circuits 104-110 (e.g. details of 104 are shown in Fig 3). As described in the Abstract, "Each sub-system...may have a separate validity circuit to individually determined if the supply voltage is adequate for that subsystem to produce a stable output signal." Therefore, after considering the figures and disclosure, one of ordinary skill in the art would recognize the circuit/means of Smith would also provide

initialization to an internal circuit when the supply voltage reaches the acceptable operational levels in accordance with a plurality of associated signals.

Response to Arguments

The applicant's arguments filed Aug 22, 2002 have been fully considered but they are not persuasive. The applicant argues: 1) the prior art does not provide "pulse signals at the time power is turned", disclose "pulse generators", nor the conversion of the comparison result "into pulse signals and outputs them"; 2) Malherbe's, and Crotty's POR circuits are different from the present invention's POR circuit; and 3) Crotty has voltage detection circuits, low pass filters, and a buffer circuit.

1) In response to the applicant's argument that the references fail to show certain features of the applicant's invention, it is noted that the features upon which the applicant relies (i.e., "pulse signals at the time power is turned on" (see the amendment, page 6); "pulse generators"/"pulse signals having waveforms (d) and (f) in Fig. 3" (see the amendment, page 8); and "pulse signals and outputs them" (see the amendment, page 8) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). For example, each of the original independent claims 1, 3, and 5 clearly recite "generating a pulse signal as a main power-on reset signal", and none of them recite "pulse generators." Therefore, one of ordinary skill in the art would know the argument's plurality of "pulse signals" is not the same as the singular "a pulse signal" recited within the claims. However, the plurality of sub power-on reset signals recited within the claims could be

considered a type of "pulse signals" being referred to within the arguments. If that is the case, both Malherbe and Crotty show circuitry that provides more than one pulse signal as the sub power-on reset signals. Related to these "pulse signals", one of ordinary skill in the art knows that circuitry that provides some type of power-on reset signal(s) (e.g. POR), will provide the appropriate POR signal(s) during initial power-up, and also when the power supply would fall below its predetermined, minimum operational level. When the power supply returns above the minimum operational level again, whether during an initial power-up phase, or as a result of a temporary power fluctuation, the circuit will still provide the proper POR signal(s) with respect to the level of the supply voltage(s).

2) The applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. For example, although the disclosed invention might be different than Malherbe's (and Crotty's) circuits in some ways, the claimed invention does not differ since the "at least one" signal(s) limitation is met by each reference of Malherbe and Crotty. It is also understood that "at least one" includes not only one signal, but two or more signals. As one of ordinary skill in the art would know, the output of an OR logic gate will be low only when all its input signals are low. For example, if two of three input signals are already low, the output will become low when the third (i.e. last one) input signal transitions to low. Similarly, if all three input signals are low, if any one of them transitions high, the output of the OR logic gate will transition high. Therefore, the pulse signal POR of Malherbe's circuit will be generated according to at least one of the

signals applied to the OR logic gate's inputs. Similarly, Crotty's NAND gate/inverter 650 (shown in Fig. 7) will provide an appropriate pulse signal POR in response to at least one of the input signals POR1, POR2. However, in the case of a NAND gate, each of the input signals must be high before the NAND gate's output can be low. If each input is high, the output will transition high if either or both of the NAND gate's inputs go low.

3) Similar to #2 above, Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections. The applicant appears to rely on how components are labeled within the prior art reference versus the actual invention claimed. For example, page 10 of the amendment recites "the power-on reset circuit of Crotty is distinguishable from the present invention because the power-on reset circuit of Crotty comprises two voltage detection circuits, two low pass filters, and a buffer circuit." However, as pointed out within the rejection's descriptions, blocks 630,640,650,210,220 closely correspond to respective blocks 10,16,20,12,18 shown in the applicant's Fig. 1, wherein Crotty's more detailed circuitry shown in Figs. 4(a), 5(a), and 7 closely correspond to blocks 16,18 and 20 of the applicant's Fig. 1. For example, the applicant's block 20 shows a NAND gate receiving two input signals (PLSH and PLSL), and providing its output signal to an inverter. Block 650 of Crotty also shows a NAND gate receiving two input signals (POR1 and POR2), and providing its output signal to an inverter. Therefore, Crotty's block 650 and the applicant's block 20 are identical, except for their identifying

labels. Similarly, the applicant's Fig. 1 shows block 16 with NAND gate 26 receiving input signal PORH directly, and indirectly through delay 22 and inverter 24. In Crotty's Fig. 4(a), NAND gate 410 receives input VD1 directly, and indirectly through delay circuit 420. However, the delay circuit is shown in detail in Fig. 5(a). One of ordinary skill in the art would know inverters 512-516 could also be considered a delay. Therefore, NAND gate 410 of Crotty does receive input VD1 indirectly through delay 512-516 and inverter 518, thus corresponding to the applicant's own block 16. Whether they are labeled differently or not, the functions of both Crotty's and the applicant's own corresponding blocks will still be the same because of their identical (or equivalent) structure.

The applicant's present arguments, and the examiner's corresponding response, closely correspond to the arguments within the amendment submitted on Feb 7, 2002, and the resulting examiner's Final Action mailed on Apr 22, 2002. Therefore, it does not appear anything new is actually being covered.

As with the applicant's Feb 7th amendment, it is noted that the applicant's arguments (e.g. on page 9 of the present amendment) specifically identifies Crotty's Fig. 2. Therefore, the applicant's arguments with respect to the Crotty reference never clearly address the specific details described within the rejection that relates to (or identifies) Figs. 3(a), 3(d), 4(a), 5(a), 6, 7, and 10. As such, it is not understood how the applicant relates Crotty's Fig. 2 to the examiner's rejections. It is suggested that if the applicant intends to traverse the examiner's rejections, the arguments should refer specifically to what the rejections clearly identify (e.g. the proper figure and elements)

with respect to what limitations are actually recited. General allegations will not overcome the rejections described within the Office Action(s).

Therefore, all the rejections described with respect to the references of Malherbe and Crotty in the previous Office Action, and also in this Office Action, are deemed proper with respect to the understanding of the claimed limitations by one of ordinary skill in the art.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE
Terry L. Englund

21 September 2002

TIMOTHY P. CALLAHAN
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